CT8224 4 Key touch

detection IC

new version	update time	Update Explanation	description
V1.3	**2015-6-18**	Important modify the application circuit (option feet vacant issue)	4 Key touch detection IC
V1.4	**2015-8-31**	Modify the three key resistance incorrect application problems	4 Key touch detection IC

I. Overview

CT8224 It is a design principle using capacitive sensing touch IC , Its stable induction may be applied to various electronic

Product, the panel can be fully insulated dielectric material, designed to replace conventional mechanical switches or a common key structure design. provide 4

Touch input pins and 4 Direct output pins.

Second, characteristics

Operating Voltage: 2.4V ~ 5.5V

It can be externally Option Select whether to enable the internal regulator circuit function

Working current@ VDD = 3V When no-load, low-power mode is typically less than the value of 4.0uA

@ VDD = 3V When, in the fast mode, the fastest response time of the touch key 60mS , Low power mode 160mS

Each touch sensitive keys degree It may be adjusted by an external capacitor (0 ~ 50pF)

provide LPMB Pin select fast mode or low-power mode

Direct output mode, trigger mode, open-drain output, CMOS Active-high or active-low output, via

TOG / AHLB / OD Select Pin

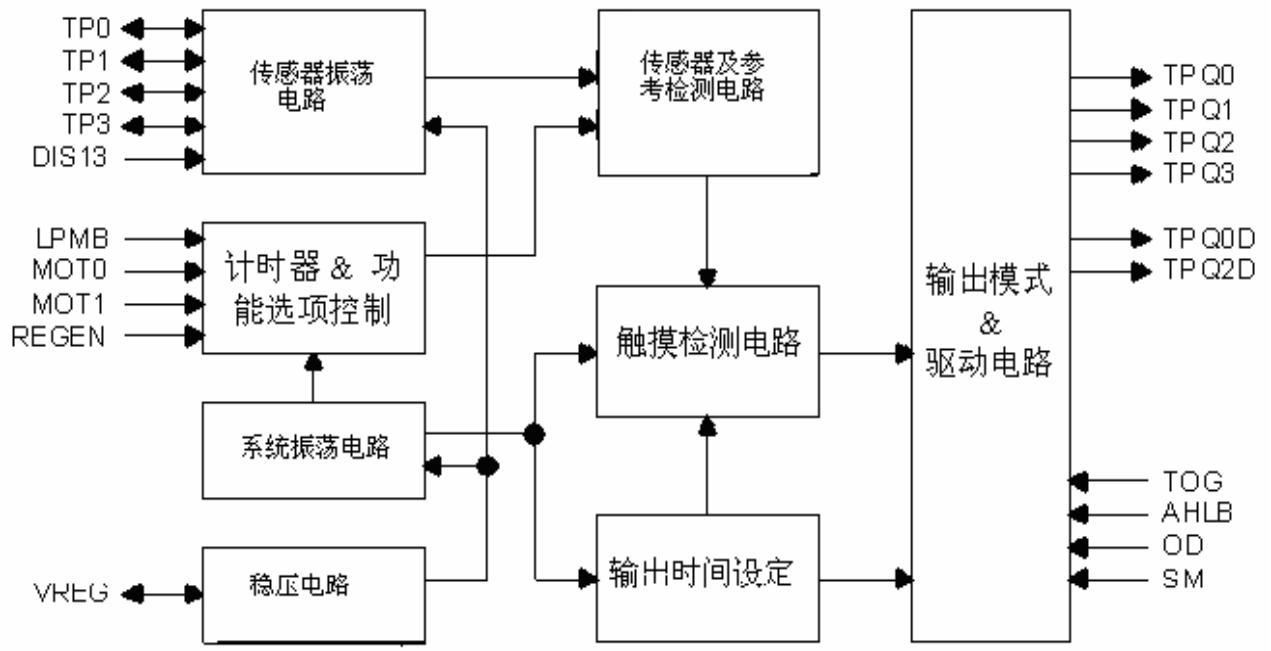
No protection diodes provide two output pins TPQ0D , TPQ2D It is limited to active low

provide MOT1, MOT0 Pin select the maximum output time: 120Sec / 64 Sec / 16 Sec / gigantic

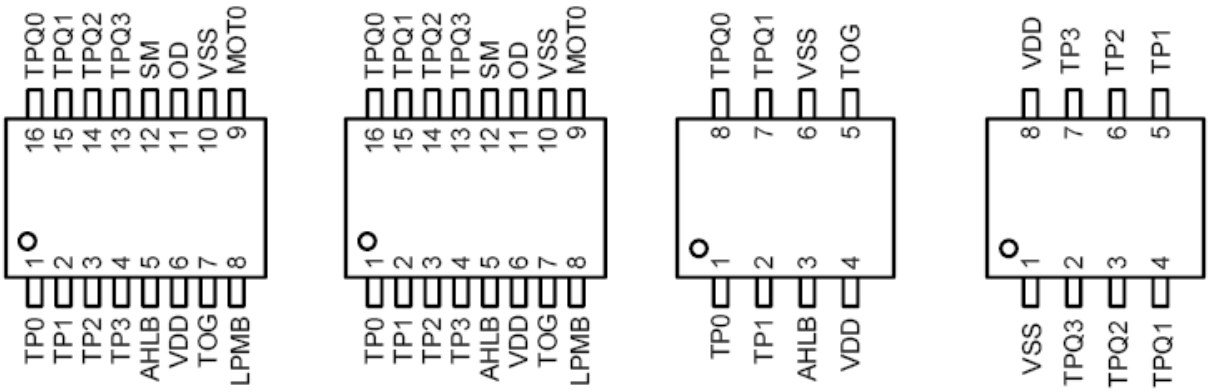
After power is about 0.5 Sec The system settling time, during this period do not touch Touch PAD And Touch does not work

Automatic calibration, when no key is touched, the system re-calibration cycle is about 4.0 Sec

Third, a functional block diagram



Fourth, the package and Pin Description



SSOP16

8224S-4 (4KEY)

SOP16

8224-4 (4KEY)

SOP8

8224-2 (2KEY)

SOP8

8224-3 (3KEY)

No.	name	I / O Types of	Functional Description
1	TP0	I / O	Touch input pin
2	TP1	I / O	Touch input pin
3	TP2	I / O	Touch input pin
4	TP3	I / O	Touch input pin
5	AHLB	I-PL	High-output, active low level to select the default value: 0
6	VDD	P	A positive supply voltage
7	VREG	P	Internal voltage regulator circuit output pin
8	TOG	I-PL	Output type selection, default: 0
9	LPMB	I-PL	Low-power / fast mode, the default value: 0
10	MOT1	I-PH	Maximum output time options: Default: 1
11	MOT0	I-PH	
12	VSS	P	Negative power supply voltage, ground
13	DIS13	I-PH	TP1 , TP3 Disable select pin, the default value: 1
14	REGEN	I-PH	Internal voltage regulator circuit enable / disable selection, the default value: 1
15	OD	I-PH	Open drain output selection, default: 1
16	SM	I-PH	Touch / multi-output selection keys, default: 1
17	TPQ3	O	Direct output pin
18	TPQ2	O	Direct output pin
19	TPQ2D	OD	Open drain output (no diode protection circuits), active low
20	TPQ1	O	Direct output pin
twenty one	TPQ0	O	Direct output pin
twenty two	TPQ0D	OD	Open-drain output (no diode protection circuits), active low

Note: Pin type, I => CMOS Input, I-PH => A pullup resistor CMOS Input, I-PL => With a pull-down resistor CMOS Input;

O => CMOS Output, I / O => CMOS input Output, P => Power / ground, OD => CMOS Open-drain (Open Drain) Output;

V. Functional Description

1. Sensitivity adjustment

PCB Sensing board pad size and wiring will directly affect the sensitivity, sensitivity adjustment according to the actual application PCB should

Adjusted CT8224 Some external sensitivity adjustment method.

1-1 Sensing changes in the size of the pad

If other conditions are fixed, using a larger pad will increase the sensitivity of sensing, sensitivity will decrease and vice versa, but the induction welding

Disc size must be within the effective range of values.

1-2 Panel thickness changes

If other conditions are fixed, the use of a thinner panel will also increase the sensitivity, the sensitivity is decreased and vice versa, but the thickness of the panel

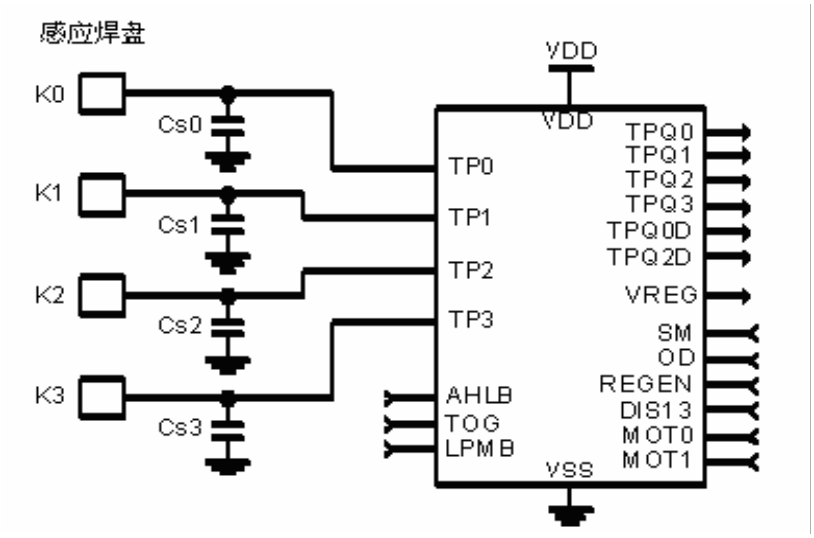
We must be less than its maximum value.

1-3 By adjusting the external capacitor Cs0 ~ Cs3 (Referring to FIG. 5-1)

If other conditions are fixed, can be adjusted according to the actual situation of each key Cs The capacitance value to reach the best sensitivity, while

That the sensitivity of each key agreement reached. when Cs When the capacitance is not connected to the highest sensitivity. Cs0 ~ Cs3 The lower the value of the tolerance sensitivity,

Cs Adjustment range: 0 ≦ Cs0 ~ Cs3 ≦ 50pF .



Map 5-1 FIG relationship with each key capacitance

2. Output mode selection (by the TOG , OD , AHLB Pin Select)

CT8224 Output pin direct output mode (TPQ0 ~ TPQ3) By AHLB To set the output pin high or low

Effective level, but also by TOG Pins to set the trigger mode, or by OD Pins to set the open drain output mode (protection diode

Circuit), additionally TPQ0D , TPQ2D Open-drain output active low and not only with a diode protection circuit. Table 5-1 And Table

5-2 .

table 5-1 Pin TPQ0 ~ 3 Option Description Table

TOG	OD	AHLB	Pin TPQ0 ~ 3 Option Description	Remark
0	1	0	Direct Mode, CMOS Output, active HIGH	default
0	1	1	Direct Mode, CMOS Output, active low	
0	0	0	Direct mode, open drain output, active high	
0	0	1	Direct mode, open drain output, active low	
1	1	0	Trigger mode, CMOS Output, power status = 0	
1	1	1	Trigger mode, CMOS Output, power status = 1	
1	0	0	Trigger mode, Power on state high impedance, active high	
1	0	1	Trigger mode, Power on state high impedance, active low	

table 5-2 Pin TPQ0D, TPQ2D Option Description Table

TOG	Pin TPQ0D, TPQ2D Option Description	Remark
0	Direct mode, open drain output active low, high impedance state on power	default
1	Trigger mode, open drain output active low, high impedance state on power	

3. Output selection valid key (by the SM Pin Select)

CT8224 accessible SM Pin single and multiple keys to select the output mode.

table 5-3 Output selection table valid key

SM	Function Description	Remark
1	Multi-key mode	default
0	Speed mode	

Multi-key mode: TP0-TP3 Can be touched while the output of two or more keys.

Speed mode: TP0-TP3 Only one key output, when a certain key is detected and output, additional 3 Touch keys will not work.

4. Valid key longest output time (by the MOT0, MOT1 Pin Select)

If the cause due to other non-normal factors the object touches the keys and the capacity to change enough to be recognized as a valid touch, it would have been fixed

For, in order to prevent the occurrence of such phenomena, so CT8224 Design of the valid key setting circuit longest output time, the maximum output of the key may be provided

Time when the object touches the time exceeds the set time, the system will return to the initialization state and stops power output until the next is touched

Time.

table 5-4 Effective key longest output schedule

MOT1	MOT0	Function Description	Remark
0	0	Maximum on time 120Sec	
0	1	Maximum on time 64Sec	
1	0	Maximum on time 16Sec	
1	1	Infinity (disable output time setting)	default

5. Fast mode and low power mode selected (by the LPMB Pin Select)

CT8224 There provide fast and low-power modes selectable by LPMB Pin selection, when LPMB Pin is connected to VDD

Time CT8224 Work in fast mode, when LPMB Pin floating or connected VSS Time, CT8224 Work in low-power mode.

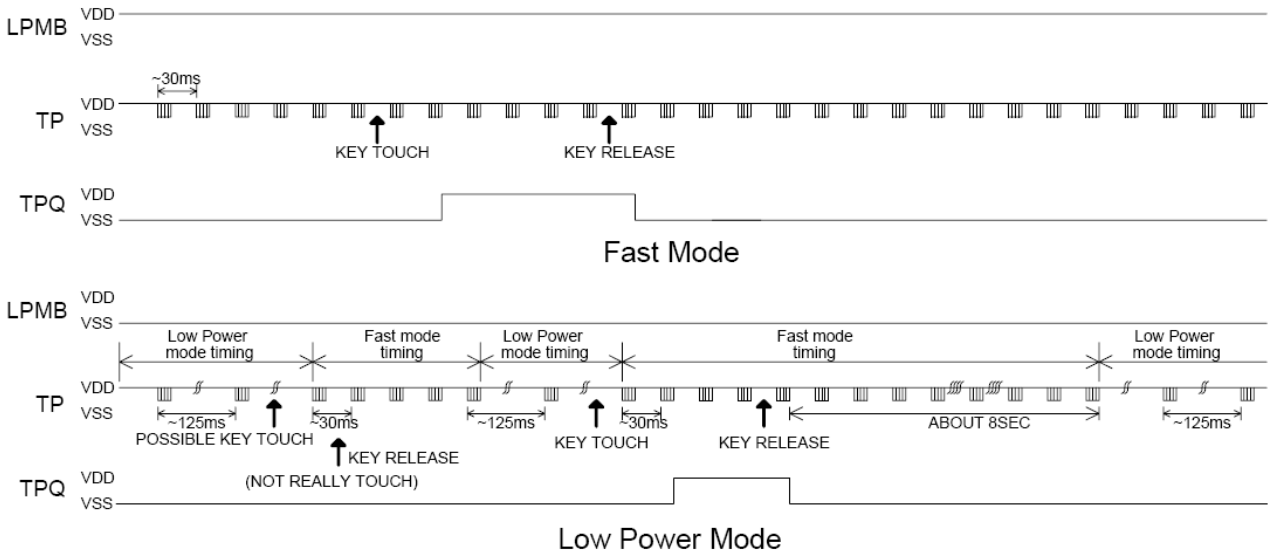
In the fast mode, faster response, but slightly larger current consumption. In low-power mode, power consumption will be smaller, but the first touch

When the response speed for work more slowly, after which the response speed is fast and patterns, so the system has automatically switched to fast mode

Make. When the key is released all over 8Sec After, turn the system back to the low-power mode. State timing shown in two operating modes 5-2 .

table 5-5 Fast mode and low-power mode selection table

LPMB	Function Description	Remark
1	Quick mode	
0	Low-power mode	default



Map 5-2 Fast mode and low power mode timing chart

6. Internal voltage regulator circuit enable / disable selection (by the REGEN Pin option)

CT8224 Internal regulator circuit, by REGEN Pins can choose whether to enable the internal regulator circuit, when REGEN Pin floating or Connected to VDD I.e., internal regulator circuit is enabled. when REGEN Pin is connected to VSS , The internal voltage regulator circuit is disabled when the disable the internal The regulator circuit, VREG Pin must external VDD Connected.

table 5-6 Internal voltage regulator circuit enable / disable selection table

REGEN	Function Description	Remark
1	Enable internal regulator circuit	default
0	Disable the internal regulator circuit	

7. To select the input key (the DIS13 Pin option)

If the key is less than two, CT8224 able to pass DIS13 Select Pin TP1 with TP3 Is disabled, in order to achieve lower power consumption. when DIS13 versus VSS When connected, touch TP1 , TP3 It is invalid.

table 5-7 Input key to select the table

DIS13	Function Description	Remark
1	Enable TP1 , TP3	default
0	Disable TP1 , TP3	

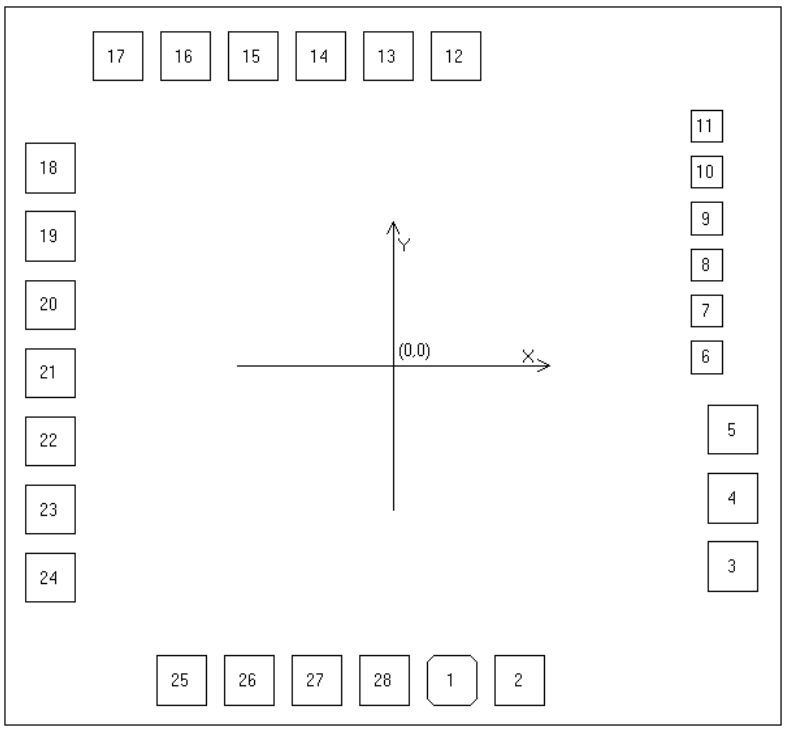
Sixth, the absolute maximum (All voltage VSS As a reference)

project	symbol	Ratings	unit
The supply voltage	V_{DD}	-0.3 to 5.5	V
Input / output voltage	V_I / V_O	VSS-0.3 ~ VDD + 0.3	V
Operating temperature	T_{DD}	0 ~ 70	℃
stored temperature	T_{ST}	--20 ~ 125	℃

Seven, electrical parameters (All voltage VSS As a reference, VDD = 3.0V , Ambient temperature 25 ℃)

parameter	symbol	condition	Min	Typ	Max	Units
Operating Voltage	VDD	Disable the internal regulator circuit	2.0		5.5	V
Operating Voltage	VDD	Enable internal regulator circuit	2.4		5.5	V
Internal regulator circuit output VREG			2.2	2.3	2.4	V
Working current(4 key, DIS = 1 , No load) I_{OP1}		Low-power mode (internal voltage regulator circuit is enabled)		3.5		μA
		Quick Mode (Enable internal regulator circuit)		8.0		μA
Working current(2 key, DIS = 0 , No load) I_{OP2}		Low-power mode (internal voltage regulator circuit is enabled)		3.0		μA
		Quick Mode (Enable internal regulator circuit)		6.0		μA
Input pin	V_{IL}	The low input voltage range	0		0.2	VDD
Input pin	V_{IH}	High input voltage range	0.8		1.0	VDD
Sink current output pin	I_{oL}	VDD = 3V, VOL = 0.6V		9.5		mA
Drive current output pin	I_{oH}	VDD = 3V, VOH = 2.4V		-5.0		mA
Key Response Time	T_R	Quick mode		60		mS
		Low-power mode		160		mS

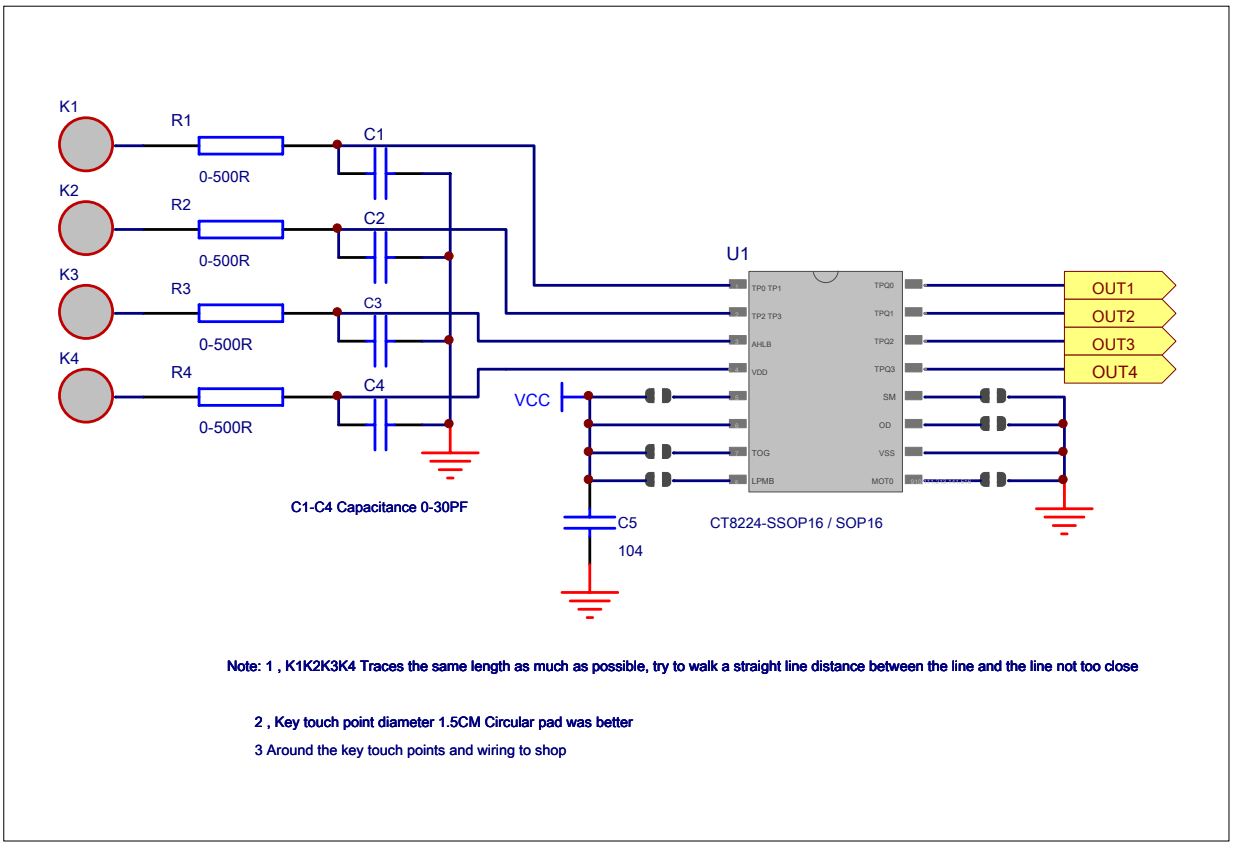
Eight, pinout FIG.



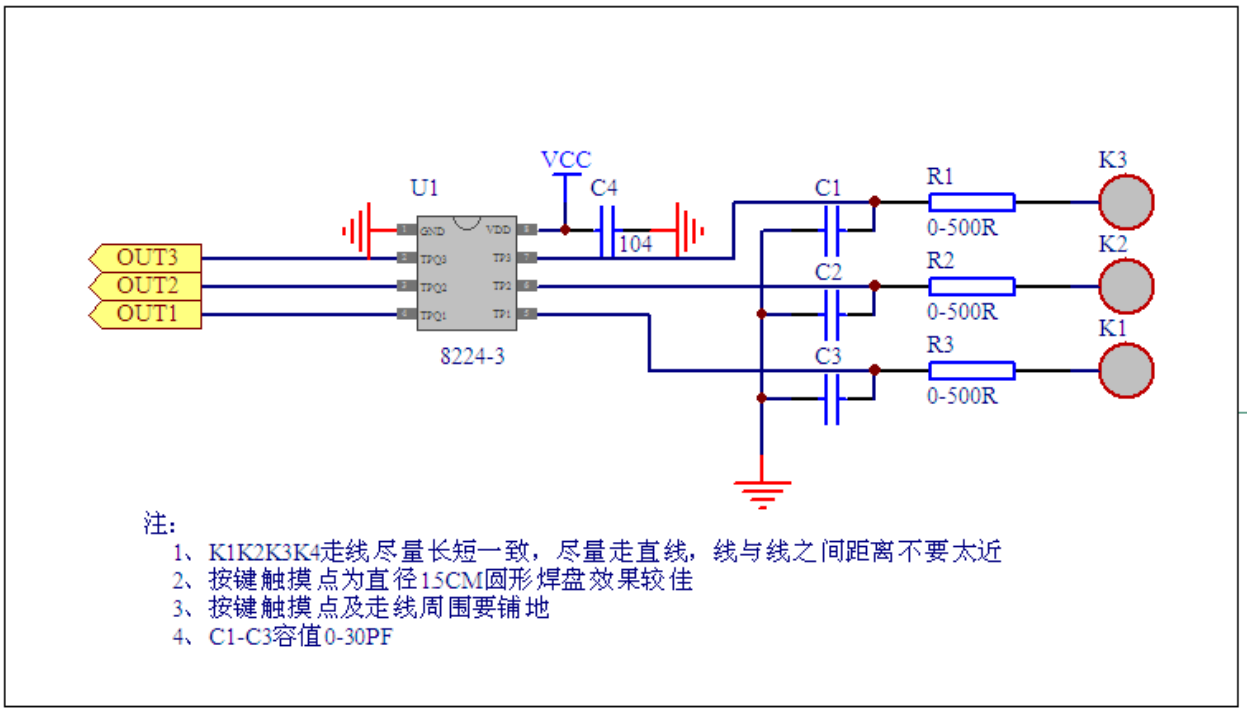
Substrate access VSS

NO.	PAD NAME	X	Y	NO.	PAD NAME	X	Y
1	TP0	103	--542	15	LPMB	--243	537
2	TP1	221	--542	16	MOT1	--361	537
3	TP2	592	--344	17	MOT0	--479	537
4	TP3	592	--226	18	VSS	--597	343
5	AHLB	592	--108	19	DIS13	--597	225
6	A	546	16	20	REGEN	--597	107
7	B	546	96	twenty one	OD	--597	--10
8	C	546	176	twenty two	SM	--597	--128
9	D	546	256	twenty three	TPQ3	--597	--246
10	E	546	336	twenty four	TPQ2	--597	--364
11	VSS2	546	416	25	TPQ2D	--368	--542
12	VDD	110	537	26	TPQ1	- 250	--542
13	VREG	--7	537	27	TPQ0	--132	--542
14	TOG	- 125	537	28	TPQ0D	--14	--542

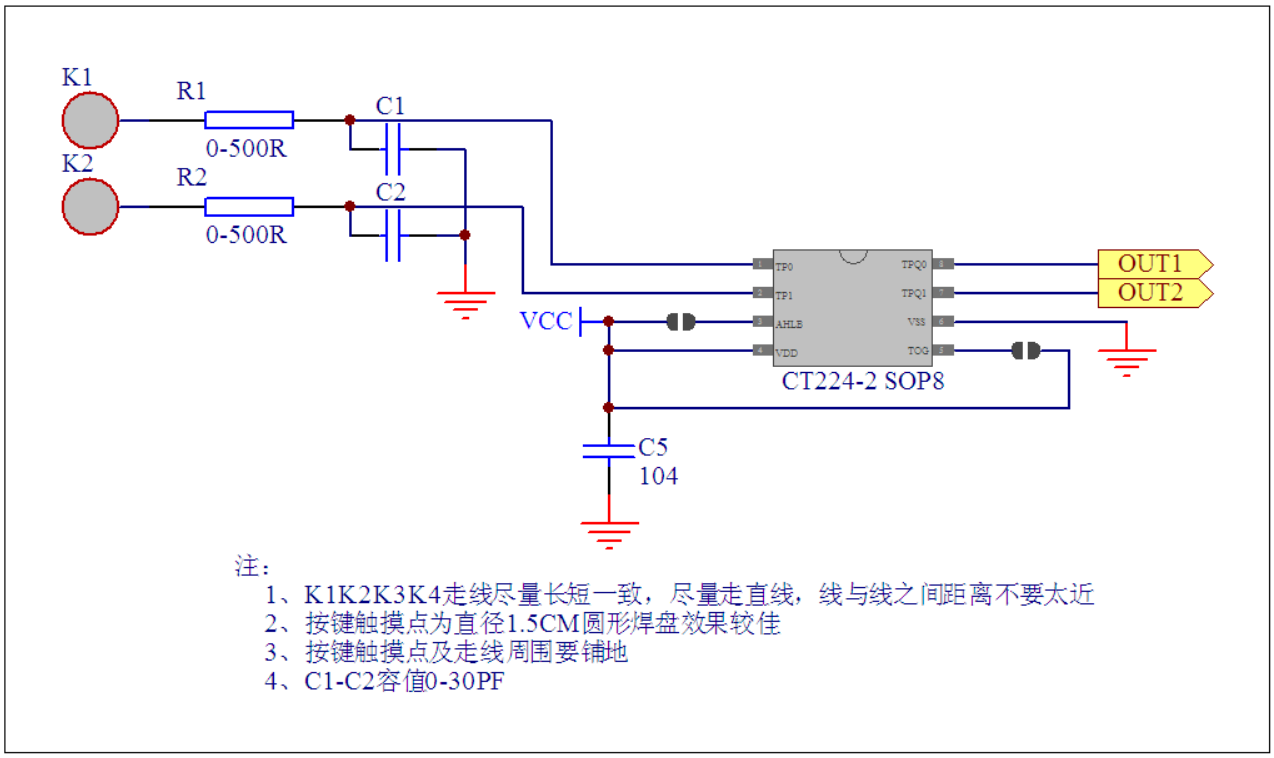
Nine, application circuit



Map 9-1 CT8224-SOP16 / SSOP16-4KEY Reference Schematic



Map 9-2 CT8224-SOP8-3KEY Reference Schematic



Map 9-3 CT8224-SOP8-2KEY Reference Schematic

输出模式说明

TOG	OD	AHLB	TPQ0-TPQ3功能说明
open	open	open	直接模式，CMOS高电平有效输出
open	open	VDD	直接模式，CMOS低电平有效输出
open	VSS	open	直接模式，开漏高电平有效输出
open	VSS	VDD	直接模式，开漏低电平有效输出
VDD	open	open	触发模式，CMOS输出，上电状态=0
VDD	open	VDD	触发模式，CMOS输出，上电状态=1
VDD	VSS	open	触发模式，上电状态为高阻抗，高电平有效
VDD	VSS	VDD	触发模式，上电状态为高阻抗，低电平有效

TOG	管脚TPQ0D，TPQ2D（无保护二极管）功能说明
open	直接模式，开漏输出低电平有效，上电状态为高阻抗
VDD	触发模式，开漏输出低电平有效，上电状态为高阻抗

键输出模式

SM	功能说明
open	多键模式
VSS	单键模式

最长输出时间设定

MOT1	MOT0	功能说明
VSS	VSS	最长输出时间120秒
VSS	open	最长输出时间64秒
open	VSS	最长输出时间16秒
open	open	无穷大（禁止输出时间设定）

快速模式\低功耗模式选择

LPMB	功能说明
VDD	快速模式
open	低功耗模式

输入键数选择

DIS13	功能说明
open	TP1，TP3启用
VSS	TP1，TP3禁用

Note: 1. in PCB , The distance sensing pads IC Connection pins as short as possible. And each of the parallel lines do not intersect.

2. Coverage PCB The panel can not be a material with a metal or other conductive components, including the outermost surface coating.

3. VDD and VSS Necessary to use a capacitor C5 Do filtering, while the wiring C5 Capacitors must be close to the closest distance IC of VDD and VSS Between the pin.

4. capacitance C1 ~ C4 It is used to adjust the sensitivity, C1 ~ C4 The smaller the value, the higher sensitivity. Sensitivity selected as needed PCB

The practical application is adjusted, C1 ~ C4 A capacitance in the range of 0 ~ 50pF .

5. The sensitivity adjustment capacitors (C1 ~ C4) It must be a good temperature stability of its capacitance, such as X7R , NPO . For touch applications,

Recommended Use NP Capacitance material to reduce the impact of temperature change due to the sensitivity.

6. R1 ~ R4 Yes Touch electrodes and a touch input resistor in series between the foot for improved touch noise immunity. If you are using environmental interference

Little, R1 ~ R4 I can not answer.

7. Peripheral PCB wiring rules specific reference "capacitive touch buttons -PCB wiring" file.

8. When the pin select options above the default value, it is recommended to the fixed level, To select the direct output mode, the TOG is recommended to pin GND.

10. Pay attention:

1. Information is subject to updating, will not further notice, please user before use to determine whether the data in hand to the latest version.

2. For the consequences of wrong or improper operation caused, we will not be liable.